Exhibit C

> between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

JX-2001 ('907 patent) at 19:2-58.

C. The Accused Products

Netlist accused many models of SK hynix's JEDEC-compliant Double Data Rate 4 ("DDR4") Load-Reduced Dual In-Line Memory Module ("LRDIMM") products of infringing the '907 patent. Final ID at 7-8. The specific accused models are listed in a table on pages 7-8 of the Final ID. *Id.*

D. The Domestic Industry Products

The asserted domestic industry articles are Netlist's 16 GC 2Rx4 DDR HV-LRDIMM and 32GB 2Rx4 DDR HV-LRDIMM. Final ID at 10. These products are specific model numbers of Netlist's Field Programmable Gate Array ("FPGA") HybriDIMM product. *Id.* at 139. Netlist has since transitioned to its Application-Specific Integrated Circuit ("ASIC") HybriDIMM product, but expressly stated that it was not relying upon that product for the domestic industry. *Id.* at 139 n.13.

II. STANDARD

With respect to the issues under review, "the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge." 19 C.F.R. § 210.45(c). The Commission also "may take no position on specific issues or portions of the initial determination," and "may make any finding or